Molded Laser fcPoP

Molded Laser fcPoP: fcVFBGA-PoPb, fcWFBGA-PoPb

Highlights

- Stacking fully tested memory and logic packages eliminates known good die (KGD) issues
- Package-on-package stacking provides flexibility in mixing and matching IC technologies
- Enables assembly of larger dies in thinner PoP stack up with top ball pitch finer than bare die option
- Enables Package-on-Package solutions with low cost BOM
- Devices can be procured from multiple manufacturing sources
- Meets accepted package and board level reliability standards for CSP

Features

- CuOSP on bottom BGA and top memory interface pads
- Die thickness down to 60µm qualified
- Supports 0.3mm minimum ball pitch on bottom/BGA pads and down to 0.3mm pitch on top memory interface pads of PoPb
- CuOSP with SOP-SAC305 or Cu pillar for flip chip pads
- Qualified and HVM in 40nm, 28nm, 16nm, and 10nm Fab node with lead-free solder or Cu pillar bump
- Both Capillary Underfill (CUF) and Molded Underfill (MUF) available
- MUF allows for increased cavity size and hence larger die size, with lower assembly cost solution
- Bottom PoP package thickness of 0.5mm max with 100mm thick flip chip die and 4 layer BU substrate
- Molded laser PoP with exposed die (ED) with 0.60mm max height package thickness qualified
- Full in-house electrical, thermal and mechanical simulation and measurement capability
- Full in-house package and substrate design capability
- Turnkey solution including wafer bumping in both lead-free solder, and Cu pillar bumps

Applications

We offer a complete PoP portfolio for a range of applications:

- PoPb: Application, baseband or multimedia processor for mobile handset and portable devices
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Our Package-on-Package (PoP) family includes a stackable flip chip BGA as the bottom PoP package (PoPb). PoPb is typically an application processor or a baseband device with land pads placed on the top periphery of the package surface to enable the stacking of a second FBGA or PoP top (PoPt) above. PoPt, with memory devices stacked within, is assembled, tested and yielded independently. The two packages are combined by reflowing together (usually performed simultaneously) on the application board to form PoP (Z-interconnection with solder ball).

PoP has emerged as the preferred approach to integrate memory and logic in many advanced mobile and handheld applications. The bottom logic package and top memory package can be assembled, tested and yielded independently. This business model is preferred by end users as they can leverage their usual suppliers for these device types independently and have the flexibility to match logic processor and memory to support different applications.

We have always been at the forefront of 3D packaging and stacked die packaging. The wirebonded bottom PoP package was developed and introduced into production years ago. The bottom fcPoP provides the advantage of denser design with larger die size and higher number of IOs within the same PoP package body size / form factor as compared to the wirebonded PoP version. In addition, the use of fcPoP allows for potentially lower PoPb package height, thus reducing the total package stacked height post-SMT process. Improved device electrical performance can also be expected with the fcPoP package as with all other Flip Chip packages in comparison to wirebonded designs.

Molded Laser PoP (PoP-MLP) allows for further height reduction and the use of tight memory interface (MI) pitch down to 0.3mm. A next-generation molded laser PoP with exposed die (PoP-MLP-ED), results in further package height reduction compared to PoP-MLP and will enable maximum package heights below 0.6mm (including warpage).

Speci□cations

Die Thickness	Minimum 60mm
FC Bump Pitch	Minimum 140mm (Pb-free) Minimum 80mm/40mm (Cu/SnAg)
FC Bumps*	Pb-free, Cu pillar
Solder Balls	Sn/Ag/Cu (Pb-free ball)
Marking	Laser
Packing Options	JEDEC tray or tape & reel

*Refer to fcCuBE datasheet for PoP package details using Cu pillar interconnect.

Reliability

Moisture Sensitivity Level	JEDEC Level 2A, (60% RH/60°C), 120 hrs
Temperature Cycling	Condition B (-55°C/+125°C, 1000 cycles)
Temp/Humidity Cycling	85°C/85% RH, 1000 hrs
Highly Accelerated Stress Test	135°C/85% RH, 96 hrs
High Temperature Storage	150°C, 1000 hrs

Thermal Performance

Thermal behavior is determined by the exact con□guration of the overall structure and the distribution of power dissipation among all of the die. During the package design process, we provide quick-turn thermal feasibility analysis and data as needed to help ensure proper thermal operation.

Package	Leads	Die Size (mm)	Power (W)	T_A (°C)	Air□ow (m/s)	T_J (°C)	θja (°C/W)
12 x 12mm PoP-MLP	753	7 x 7 x 0.1	2	25.0	NC**	70.7	22.8
14 x 14mm fcPoP-MLP	641	8 x 8 x 0.1	2	25.0	NC**	68.7	21.8
15 x 15mm fcPoP-MLP	1206	11 x 12 x 0.07					

Notes: *Typical bottom molded laser fcPoP package thermal performance. Data for bottom PoP only without the e□ect of top PoP package. Substrate 4 layer laminate build-up (1/2/1). Simulation data for package mounted on 4 layer PCB per JEDEC JES51-9 under natural convection. **NC=Natural Convection

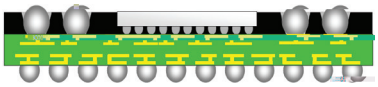
Electrical Performance

The electrical behavior is highly dependent on the package layout and the substrate structures. 3D electrical simulation is used to predict the actual electrical behavior once designs are partially or fully completed. As expected, the electrical performance advantage of using □ip chip over wire bond is seen in these packages.

Cross Sections

Bottom fcPoP (PoPb)

Molded Laser fcPoP

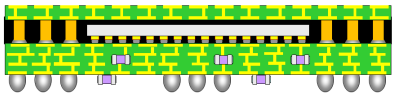


Molded Laser fcPoP with exposed die (ED)

Pre-Stacked fcPoP (PoPb + PoPt)

Molded Laser fcPoP

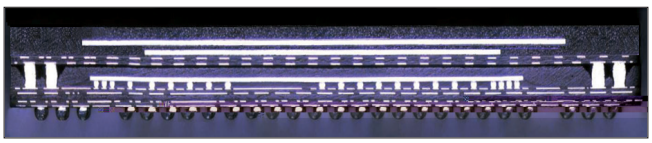
Molded Laser fcPoP with exposed die (ED)



Interposer fcPoP

Package Con□gurations

Package	Wire Bond	Flip Chip	Body Size (mm)	BGA Pitch (mm)	Top Pitch (mm)
PoP-MLP	Yes	Yes	10x10 ~ 15x15	min 0.4mm	0.4 ~ 0.5
PoP-MLP-ED	No	Yes	10x10 ~ 15x15	min 0.4mm	0.4 ~ 0.5



fcFBGA-PoP-MLP

Reference data:
PoP-MLP < 0.5mm maximum
PoP-MLP-ED < 0.6mm maximum

Test Services

- Product Engineering support
- Probe capability
- Program generation / conversion
- Drop shipment available

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